IN THE SPECIFICATION

Please add the following description of FIG. 14 which was added as suggested by the Examiner to make the drawings conform to the Specification and the Claims. Since FIG. 14 places elements found separately in FIGS. 1-6 and described in the Specification, the Applicants have added additional detailed description of added FIG. 14.

Please insert the following paragraphs beginning on page 33, line 21:

FIG. 14 is a block diagram of circuit elements described relative to FIGS. 1-13 and in particular to FIGS. 1-6. SRB 212 comprises a plurality of registers (in this case 64 registers). The registers are partitioned into a plurality of data entry fields: Valid bits 601, Instruction ID 602, Instruction Status 603, Load/Store 604, Real Address 605, and Quadword 607. Since there are 64 registers in SRB 212 there are 64 data entries in each data entry field (e.g., Real Address (0)-Real Address (63)). Address Generator generates the addresses 1516 used to access SRB 212. Data entries corresponding to register addresses (0-63) may be updated (add data) or removed (deleted). Registers of the SRB 212, according to embodiments of the present invention, are addressed by the use of pointers. Pointers contain the addresses of the registers in the SRB 212. Particular pointers, for example, the IN pointer 615 and the OUT pointer 614, are loaded with particular register addresses which are indexed under certain conditions. The IN pointer 615 points to the register where a register entry is next added and OUT pointer 614 points to the register where a register entry is next retired or removed.

Operations of the SRB are performed by special circuitry called filters. Filters, according to embodiments of the present invention, are uniquely associated with each service (operations that are performed on data entry fields). All filters operate in parallel, checking to determine whether there is any entry that needs the particular service of the filter, selecting the earliest entry if there are several, and dispatching that entry to the hardware that performs the service. The filters also perform the operation of "scanning" the entry fields of the SRB 212. Scanning may be done with a multiplexer or other circuit that allows a predetermined input value (e.g., a real address) to be compared to a

value in like data entry fields (e.g., Real Address fields 605 ) in the SRB 212 registers to determine a match. On a match, the address of the register containing the matching value is compared to the register addresses bounded by register address pointers (e.g., IN pointer 615 and OUT pointer 614). Operations may be performed on data entry fields of a register corresponding to a matching value as a result of scanning based on a decode of other data entry fields (e.g., Instruction Status field 605).

FIG. 14 illustrates circuitry employed in a filter. For example, Real Addresses 605 are coupled in parallel to multiplexer (MUX) 1511. A scan signal 1517 produces each Real Address (0-63) stored in data entry field 605 as a sequential output of MUX 1511. To determine if a particular Real Address 1514 is in SRB 212, comparator 1512 compares input Real Address 1514 to the scanned Real Addresses 605. In this example, MUX 1511 decodes addresses (0-63) to produce the required signals internal to MUX 1511 that sequentially selects the stored Real Addresses (0-63). If comparator 1512 determines the input Real Address 1514 matches with a stored Real Address 605, then a compare signal 1513 is generated that latches the scan signal value (register address corresponding to the compare 1513) into latch 1509 which is outputted as Match Address 1508. Match Address 1508 is the register address (0-63) which has the Real Address 605 that matches the input Real Address 1514. An address comparison circuit compares MA 1508 with IN Pointer (Ptr.) 615 (address) and the OUT Ptr. 614 (address) to determine if MA 1508 indicates that the register corresponding to MA 1508 is in a register whose address lies between IN Ptr. 615 and OUT Ptr. 614. Entries in registers between IN Ptr. 615 and OUT Ptr. 614 have valid entries as indicated by Valid bit 601.

If a Real Address 605 matches input Real Address 1514 and it is in a register located between IN Ptr. 615 and OUT Ptr. 614, then MA 1508 is outputted as gated MA 1504 to Address Generator 1505 which outputs the data entry fields of the register with the address corresponding to MA 1504. In this example, the Quadword 607 in the register (0-63) of SRB 212 corresponding to MA 1504 is dispatched to an operation unit (e.g., IMU 102) in response to a decode of data in the Instruction Status 603 entry by decoder 1503. Other operations may be done on data entry fields (e.g., 601-605) of a

register corresponding to a matching values as a result of scanning based on a decode of other data entry fields. Since the operations to be performed on data in each of the SRB registers is contained within the fields of the registers, the SRB has a "data flow" architecture. More detailed operations of the SRB are explained relative to the state diagrams of FIGS. 7-12. FIG. 14 only shows scanning being implemented on the Real Address 605 data entry field. It is understood that any of the particular data entry fields shown in FIG. 14 or other data entry fields not shown in this example of FIG. 14 may employ the data flow architecture with filters operating in parallel to scan the data entry fields.